PLL EMPLOYING A SAMPLE-BASED CAPACITANCE MULTIPLIER

ABSTRACT OF THE DISCLOSURE

A phase detector (PD) generates an up/down signal based on the phase error between data and clock signals input to the phase detector. A voltage controlled oscillator (VCO) generates the clock signal. The up/down signal is applied to a proportional charge pump and a truncated version of the up/down signal is applied to an integral charge pump. The proportional charge pump generates a first voltage for a first time period across a resistor based on the up/down signal, while the integral charge pump generates a second voltage for a second time period across a capacitor based upon the truncated version of the up/down signal and the sampling rate of the data signal by the PD. The second time period is less than the first time period. The first and second voltages are combined and applied to the VCO to drive the clock signal to synchronization with the data.